A Power-Efficient 33 GHz 2:1 Static Frequency Divider in 0.12-μm SOI CMOS

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***Abstract* — A 2:1 static frequency divider was fabricated in a 0.12-μm SOI CMOS technology. The divider exhibits a maximum operating frequency of 33 GHz. When the power consumption is scaled down to 2.7 mW, a maximum operating frequency of 25 GHz is measured.**

I. Introduction

High-speed static 2:1 frequency divider circuits are required for many applications, from frequency synthesis in wireless communications, to quadrature signal generation and clock recovery in high-speed serial links. These applications require high speed, low power, high sensitivity and monolithic integration. To date, mainly bipolar and III-V technologies employing the Current-Mode Logic (CML) style have been used to fabricate frequency dividers, due to the high performance requirements of communications systems. For example, an 87 GHz InP DHBT static frequency divider was published [1], though the 700 mW power consumption prohibits a high level of integration. CMOS technologies are now being used, though at lower speed: a CMOS static frequency divider achieved a maximum operating frequency of 18.5 GHz [2], at a power consumption of 27 mW per MSFF. Technology scaling, and materials innovations such as SOI, promise to improve the performance of CMOS frequency dividers. The impact of SOI on digital CMOS power and speed is well demonstrated [3, 4, 5]. In this paper we present the impact of an advanced SOI technology on the power consumption and speed of a CML divider-by-two.

II. Circuit Design

Figure 1 shows the block diagram of the 2:1 static frequency divider. It is based on CML master and slave latches connected in series. All the signals are differential, though the latches would also function with a single-ended clock. It can be shown that the cross connection between the output of the slave latch and the input of the master causes the clock frequency to be divided by two. The static frequency divider by 2 is usually the slowest function because of the feedback loop used. The divider is further slowed by the load presented by the output buffer to the slave latch. The latches and the output buffer are biased through current mirrors. The latches and the output buffer have a separate power supply connection so that the latches' current consumption can be monitored.

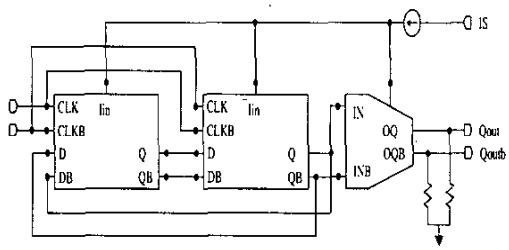

Fig. 1. Static frequency divider block-diagram

As shown in Fig 2 each latch is implemented in a classic CML architecture. Following circuit optimization, the widths of the clock and data differential-pair NFETs were designed to be 30 μm and 10 μm, respectively. Even though low-Vt NFETs are available in the technology, regular Vt NFETs were used because of the transistor matching concern. Poly silicon resistor loads of 400 Ω were used in the latches. This is a rather high load for high frequency applications [2], and it reflects the small device sizes we were able to employ because of the low drain parasitic capacitance of SOI technology.

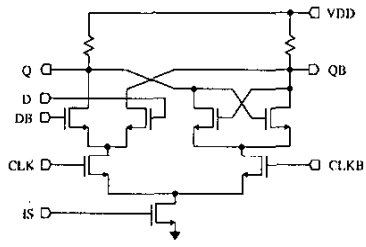

Fig. 2. Latch circuit schematic

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The small device sizes decrease power consumption, but make a 400 Ω load-resistor necessary to maintain a 700 mV peak-to-peak voltage swing. The minimum device sizes are determined by the parasitic capacitances that do not scale with device width, and also by differential-pair matching. No inductive peaking was used to extend the bandwidth frequency. The current biases of the latches and the output buffer current bias are set by current sources controlled by a current mirror. Despite the power losses, current sources are necessary in many applications for temperature compensation or to allow switching between standby and active modes. The output buffer is a differential FET pair loaded with on-chip 50 Ω resistors. The output buffer power can be set independently of the divider core by changing the independent voltage supply VDD. The schematic is given in figure 3.

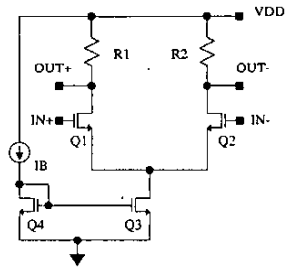

Fig. 3. Buffer schematic used for the simulation

III. TECHNOLOGY

The circuits are fabricated in a 0.12μm IBM SOI CMOS technology with 8 copper metal layers. The chip size is 0.35x0.25 mm² including the 4 RF input and output pads. We fabricated the dividers on a Regular-Resistivity Substrate (RRS) and on a High-Resistivity Substrate (HRS) with resistivities of 12 Ω.cm and 100 Ω.cm respectively.

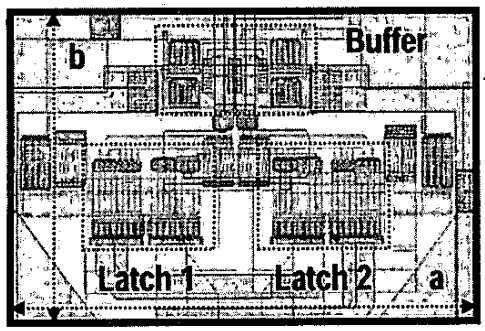

Fig. 4. Divider core layout view (a = 70μm and b = 40μm)

The manufactured NMOS transistors have a cut of frequency of 150 GHz and more than 200 GHz for the current gain (f_T) and maximum available power gain (f_{max}) respectively [5]. The technology offers a wide variety of high-Q passives such as inductors (Peak Q>50), accumulation varactors, and interdigitated back-end and MIM linear capacitors. The technology offers polysilicon resistors as well. Owing to the tight ground-rules of the technology the circuit layout, shown in figure 4, is very compact. The total area is 40 μm x 70 μm.

IV. EXPERIMENTAL RESULTS

The divider was measured at various power supply voltage biases. As shown in figure 5, a maximum division frequency of 33 GHz was measured at 2.4 V. Since three transistors are stacked between Vdd and ground, we can use voltage supply as high as 2.6 V without compromising the transistors' reliability.

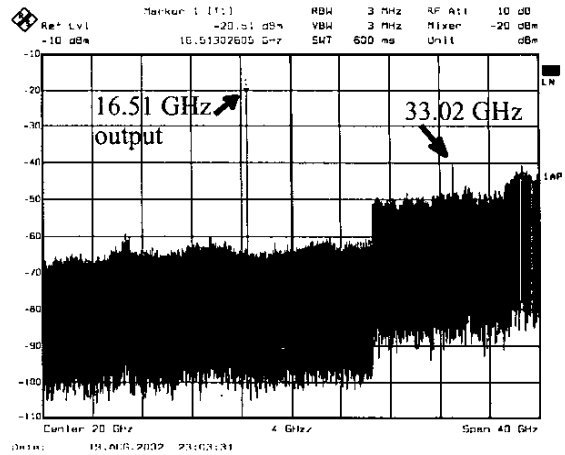

Fig. 5. Divider output spectrum measurement in a span of 40 GHz, for a 33.02 GHz input signal.

To the authors' knowledge, this is the fastest reported static frequency divider fabricated in a CMOS technology. As expected with a static divider, the circuit functions properly at low frequency (Fig. 6).

The minimum input power required to insure proper frequency division (circuit input sensitivity), as function of frequency was measured for four different supply voltages 1, 1.5, 2 and 2.4 V (Fig. 6). The maximum operating frequencies achieved at 1, 1.5, 2 and 2.4 V are 25, 28.6 30 and 33 GHz respectively. The best reported static CMOS divider has a maximum operating frequency of 18.5 GHz at 1.5V supply [2], and requires an input power of 10 dBm (Fig. 6). Figure 6 shows that the divider natural oscillation

frequency is twice as high at the same 1.5 V power supply voltage for SOI than for bulk.

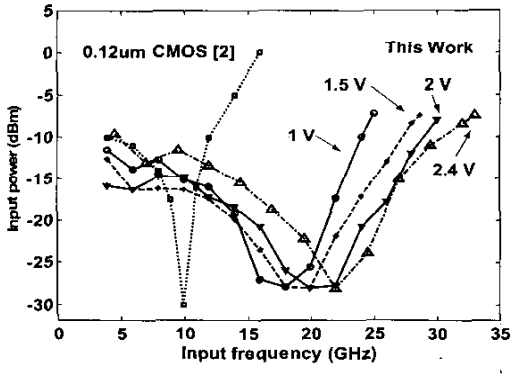

Fig. 6. Sensitivity versus frequency of static CML frequency divider-by-2 for different supply voltages

The performance advantage of SOI over bulk technology is largely aided by the absence of reverse body effect in SOI. Even though several devices are stacked in the CML frequency divider, in SOI these devices do not suffer from Vt increases. The SOI CML frequency divider is also more sensitive at maximum frequency than the bulk version.

Figure 7 shows the impact of substrate resistivity on the circuit input sensitivity. We measured the dividers with 1.0 V supply for low power circuit applications. The circuit sensitivity on HRS is several dB higher than on RRS. In high frequency applications, the substrate losses result in leakages and circuit performance degradations. The HRS provides also better isolation [7]. Overall, we measure consistently better circuit performances with HRS than RRS.

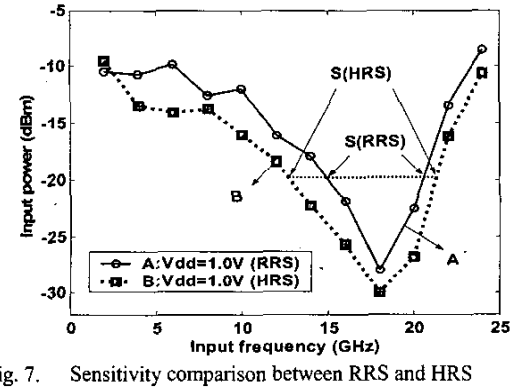

Fig. 7. Sensitivity comparison between RRS and HRS

Fig. 8 shows the maximum operating frequency as function of power consumption. The maximum operating frequency of 33 GHz is achieved at power consumption of 22.1 mW per MSFF from a 2.4 V supply. At 1, 1.5 and 2 V supply a maximum operating frequency of 25, 28.6 and 30 GHz is achieved for a power consumption of 2.7, 7.66 and 12 mW per MSFF respectively. This shows the power scalability of the SOI technology to very low-voltage operation. The fastest CMOS 0.12 μm frequency divider by 2 using the same CML latch architecture without inductive peaking operates up to 18.5 GHz, for an input power of more than 10 dBm, with a power consumption of 27 mW per MSFF from a 1.5 V supply [2].

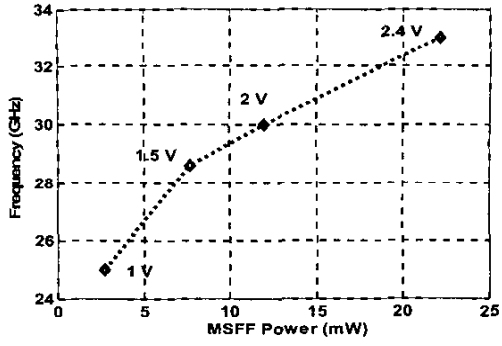

Fig. 8. Maximum operating frequency versus MSFF power consumption

One way to compare the power and speed performances of different circuit dividers is to compute the power delay product. At 1 V the SOI divider exhibits a record energy per gate of 13.5 fJ, assuming 2 gates delay per flip-flop and an equivalent complexity of 4 logic gates [6]. Fig. 9 shows a comparison of state of the art static dividers in several technologies.

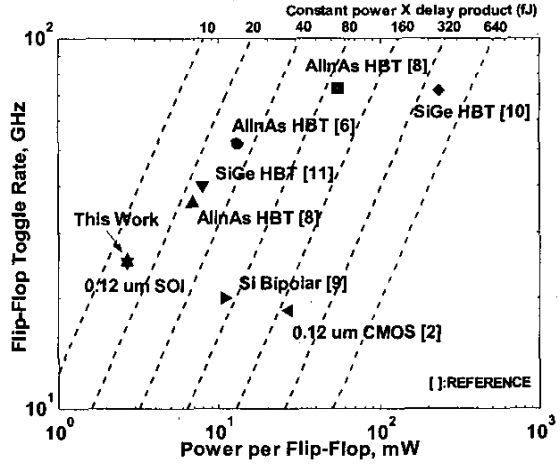

Fig. 9. Power-delay product of state of the art static dividers

This is to the authors' knowledge, the lowest static divider energy reported for any technology at a higher operating frequency than 20 GHz. The closest energy is 24 fJ for an AlInAs HBT technology, which is a 78 % higher energy than that reported in this work. The mechanism for energy reduction is very different for an SOI CMOS technology than for an HBT compound technology. Owing to the threshold and supply voltage scaling, low-operating voltage supply can be used. This allows dramatic reduction of switching energy. If we compare to bulk CMOS, the lower parasitic capacitance offered by the SOI technology is an important factor for power consumption reduction. These results combined with the ULSI capabilities of the technology are very promising for the integration of multiple high-speed serial links on the same chip. This integration could lead to the aggregation and processing of unsurpassed amounts of data.

Fig. 10 shows the chip microphotographs and the input and output access coplanar wave-guides.

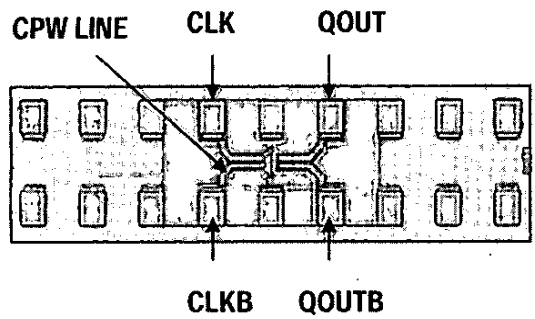

Fig. 10. Divider microphotograph

V. Conclusion

A low-power and high-performance CML static frequency divider was designed in 0.12 μm SOI CMOS technology. At 1 V a maximum operating frequency of 25 GHz was measured for a power dissipation of only 2.7 mW per MSFF. This is equivalent to a power delay product of 13.5 fJ. This is the lowest energy reported for any technology for any static divider operating at a frequency higher than 20 GHz. At 2.4 V a record 33 GHz operating frequency for CMOS technology is achieved. This demonstrates the speed and power advantages of SOI technology for CML latches used extensively for RF and high-speed communications.

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